A Resilience Roadmap

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Motivation

- Document current trends in various resilience components to better motivate R&D priorities.
  - In the context of this CCC study.
- Identify problems, potential solutions, future gaps.
  - Guided by ITRS methodology.
  - Focus on technology, devices and base circuits.
- Target: ITRS Design Chapter.
  - Timeframe: next ITRS update (late '09).
- Make results and methodology reproducible.
  - Open source the scripts and models.

Team and Proposed Roles

- Juan-Antonio Carballo (IBM), Andrew Kahng (UCSD).
  - ITRS coordination.
- Larry Wissel (IBM).
  - Provide extrinsic noise models.
- Kevin Cao (ASU).
  - Provide technology models.
- Nikil Mehta (Caltech).
  - Run simulations.
- Chris Wilkerson (Intel).
  - Sanity checks.
- Sani Nassif (IBM).
  - Overall coordination, provide intrinsic noise models.

Current Status (10/29/2009)

- PTM models for 45, 32, 22, 16 and 12nm.

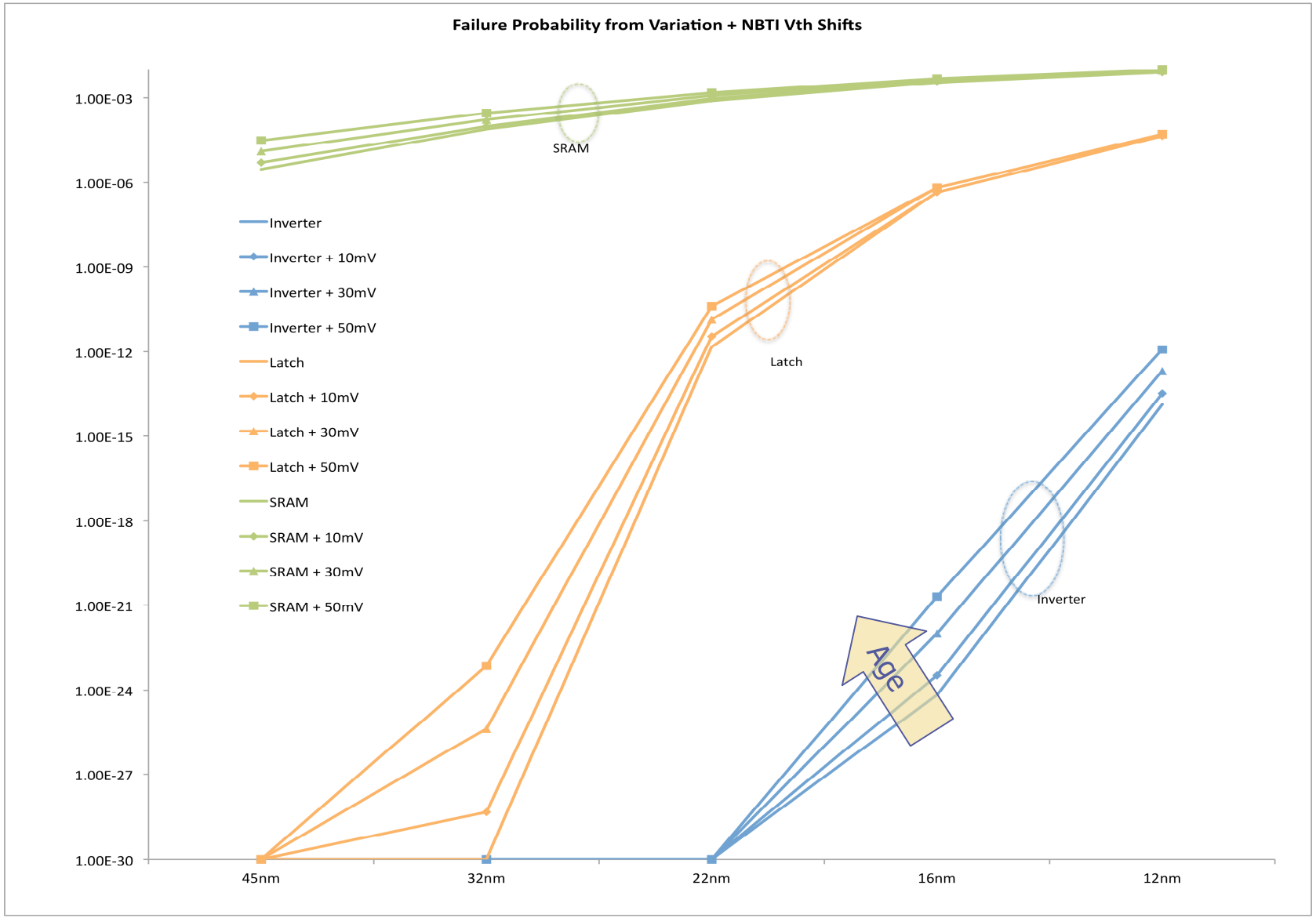
Scripts generated for:

  - Inverter
  - SRAM
  - SRAM + Noise (not detailed here)
  - Latch

- Initial runs performed to show scripts work.

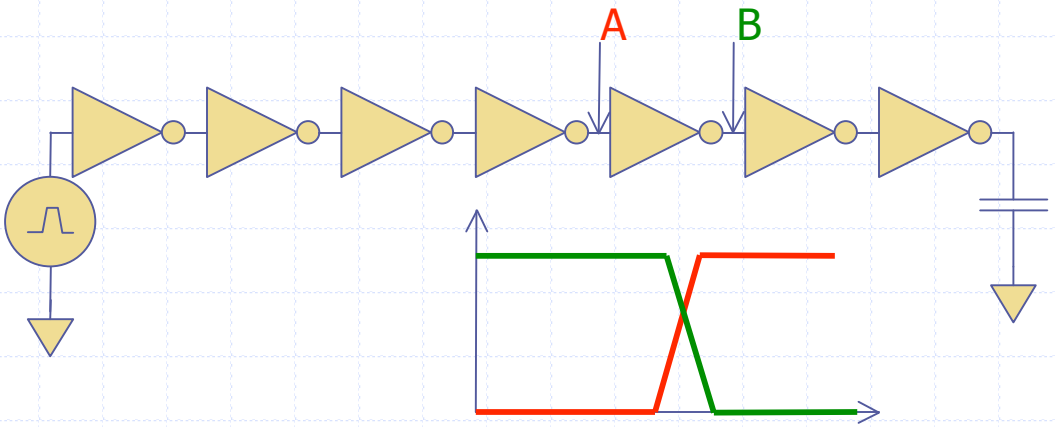
- ITRS document generated, underwent 1st review, positive feedback.

Current Results



Basics: P to N Ratio

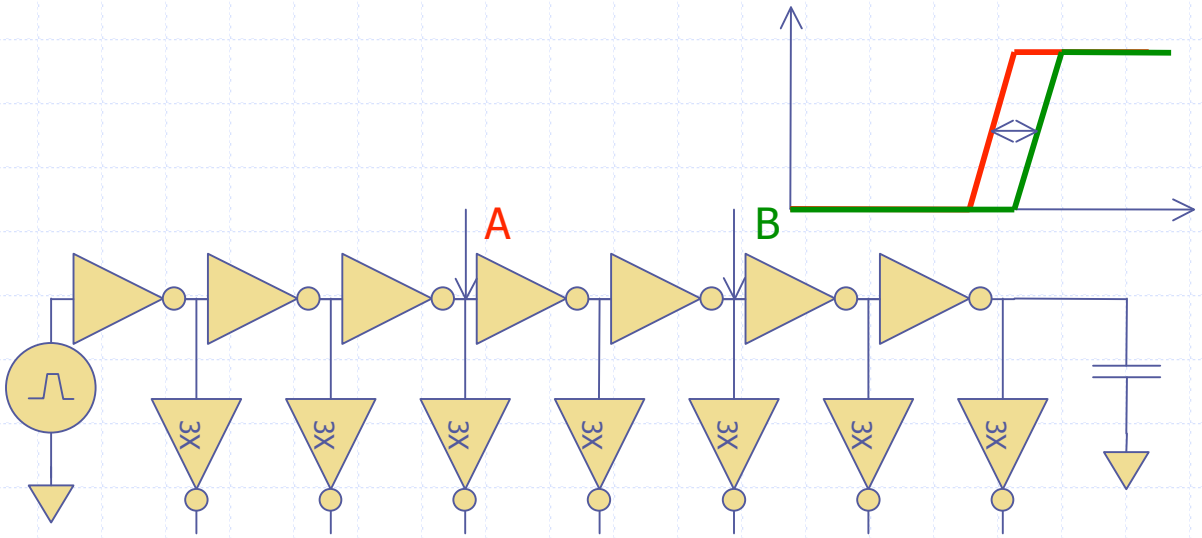
- Goal: find correct P to N ratio so that rise and fall times are approximately equal.
  - Used in other scripts to determine ratios.
- Methodology: create a string of 7 inverters, measure rise/fall times in the middle, adjust ratio to make them equal.



Technology	P/N Ratio
45nm HP	1.72
32nm HP	1.90
22nm HP	1.96
16nm HP	2.22
12nm HP	2.13

Basics: Pair Delay

- Goal: find pair delay of FO4 chain of inverters.
  - Used to set various pulse widths, rise/fall times etc…
- Methodology: create a string of 7 FO4 inverters, measure delay of 2 inverters.



Technology	Pair delay (ps)
45nm HP	22.63
32nm HP	19.59
22nm HP	17.76
16nm HP	16.07
12nm HP	15.86

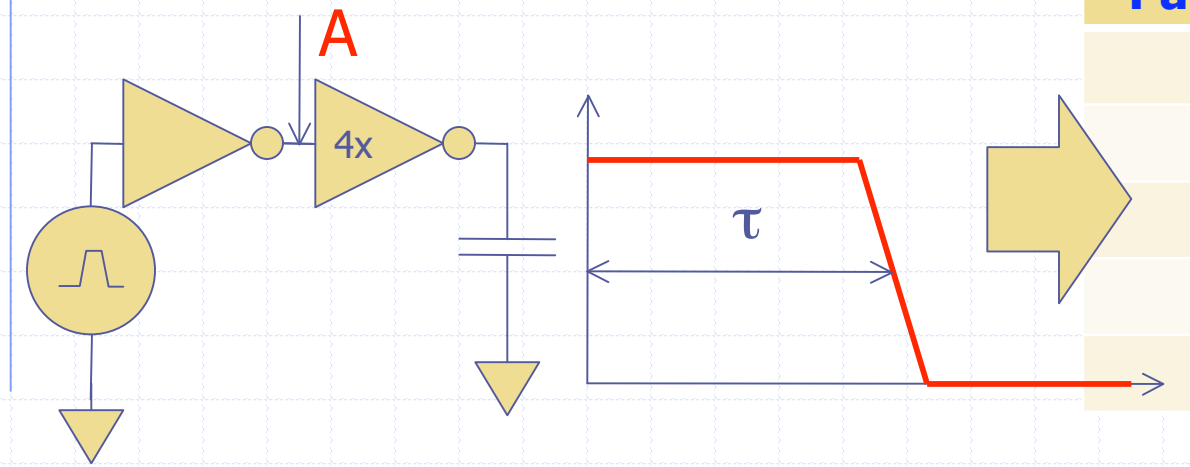
Inverter

- Goal: find failure point for inverter.
- Failure = no pulse propagation.
- Metric: fall time in a string of inverters.

Methodology:

1. Find sensitivity of metric to variations in ΔL, V_{THN}, V_{THP}, U_{0N}, U_{0P}. (by perturbing each parameter and monitoring the sign of the change in the metric).
2. Move parameters in direction to make metric worse.
3. Use bisection to find point at which failure occurs.

Methodology in Pictures



Parameter	Sensitivity
XL	+1
VTN	+1
U0N	−1
VTP	+1
U0P	+1

- Sensitivity is independent of any distributional assumptions on parameters (i.e. μ and σ).
- Failure σ does depend on distributions, so script expects user to specify the σ's.

Inverter Results

Technology	Sigma L (nm)	Sigma VT (mV)	Sigma U (as % of μ)	Failure Sigma
45nm HP	3.0	23	3	X
32nm HP	2.0	33	3	X
22nm HP	1.5	48	3	X
16nm HP	1.0	66	3	11.4
12nm HP	0.8	88	3	8.26

- X means sigma too large to estimate accurately. (probability is basically zero).
- Results are consistent with previously observed trends.
- Adjusting the Sigma values has the expected impact on the failure Sigma.

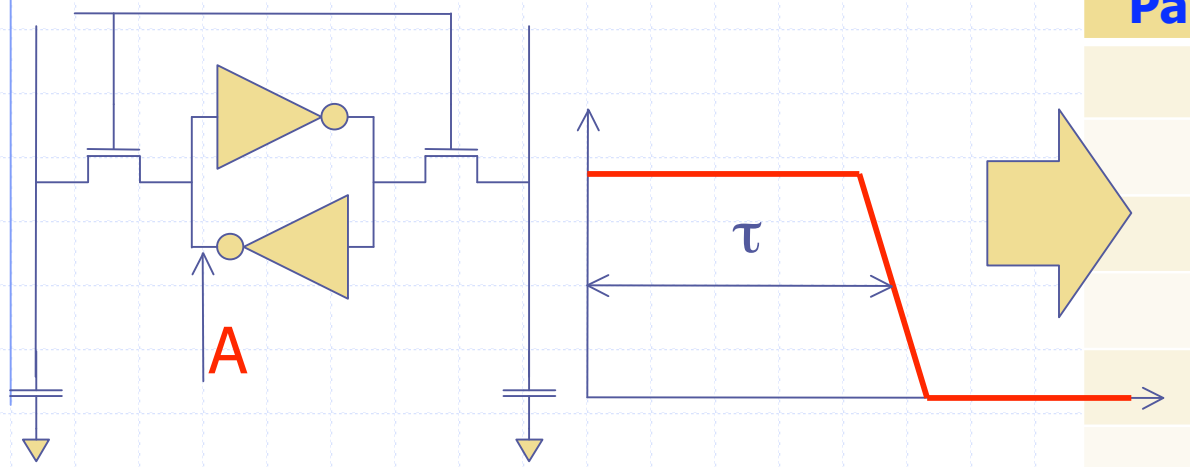
SRAM

- Goal: find failure point for an SRAM cell.
- Failure = unable to write to cell.
- Metric: delay to internal node changing value.

Methodology:

1. Find sensitivity of metric to variations in ΔL, the V_{TH} of each device, U_{0N}, U_{0P}. (by perturbing each parameter and monitoring the sign of the change in the metric).
2. Move parameters in direction to make metric worse.
3. Use bisection to find point at which failure occurs.

Methodology in Pictures



Parameter	Sensitivity
XL	+1
VTN1	+1
U0N	−1
VTP1	+1
U0P	+1
VTN2	−1
VTN3	+1
VTP2	−1
VTN4	+1

SRAM Results

Technology	Sigma L (nm)	Sigma VT (mV)	Sigma U (as % of μ)	Failure Sigma
45nm HP	1.0	47	3	6.64
32nm HP	0.6	66	3	5.47
22nm HP	0.4	96	3	4.57
16nm HP	0.3	133	3	3.93
12nm HP	0.2	177	3	3.68

- Sigma L reduced (because of SRAM regularity)
- Sigma VT increased (because of device size)

Status

- First version completed and reviewed.
  - Lots of potential remains for a more detailed study.
- ITRS design chapter was amended with a resilience section.
  - Currently in the DFM section.
  - Will separate as more material is generated.
- Prof. Cao will host the scripts, documents, and models as part of the PTM web site.
  - Release target date yet to be set.