



# A Resilience Technology Roadmap

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# Purpose/Motivation

- ◆ Document current trends in various resilience components to better motivate R&D priorities.
  
- ◆ Identify problem areas, potential solutions, and future gaps.
  - Guided by ITRS methodology.
  - Focus on technology, devices and base circuits.
  
- ◆ Target: ITRS Design Chapter.
  - Timeframe: late August 2009.

# Topic Map

Starting point...

## ◆ Taxonomy of types of failures:

- Permanent vs. Transient.
- Time (early life, useful life, end of life).
- Intrinsic vs. Extrinsic (e.g. SER) sources.

## ◆ Taxonomy of responses:

- Process/Manufacturing/Materials.
- Circuit innovation (e.g. 8T SRAM).
- Micro-Architectural innovation (eventually, not now).

# Team

- ◆ Juan-Antonio Carballo (IBM).
- ◆ Larry Wissel (IBM).
- ◆ Kevin Cao (ASU).

Not yet confirmed:

- ◆ Dennis Sylvester (Michigan).
- ◆ Looking for others...

# Mechanics

- ◆ Team will have a regular weekly phone meeting in the July/August time frame.
- ◆ Collaboratively produce text and tables needed for ITRS.
- ◆ Result will be shared with larger vision study team, as well as the ITRS design chapter leads.

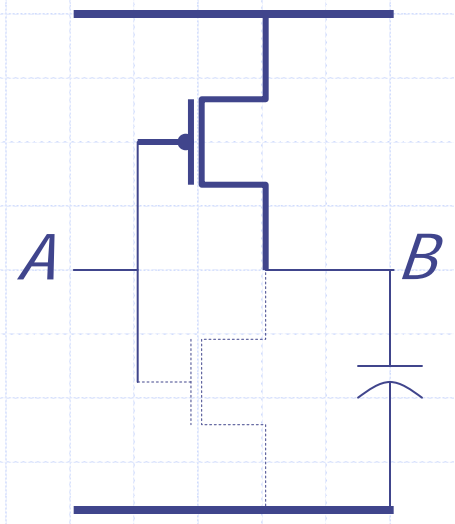
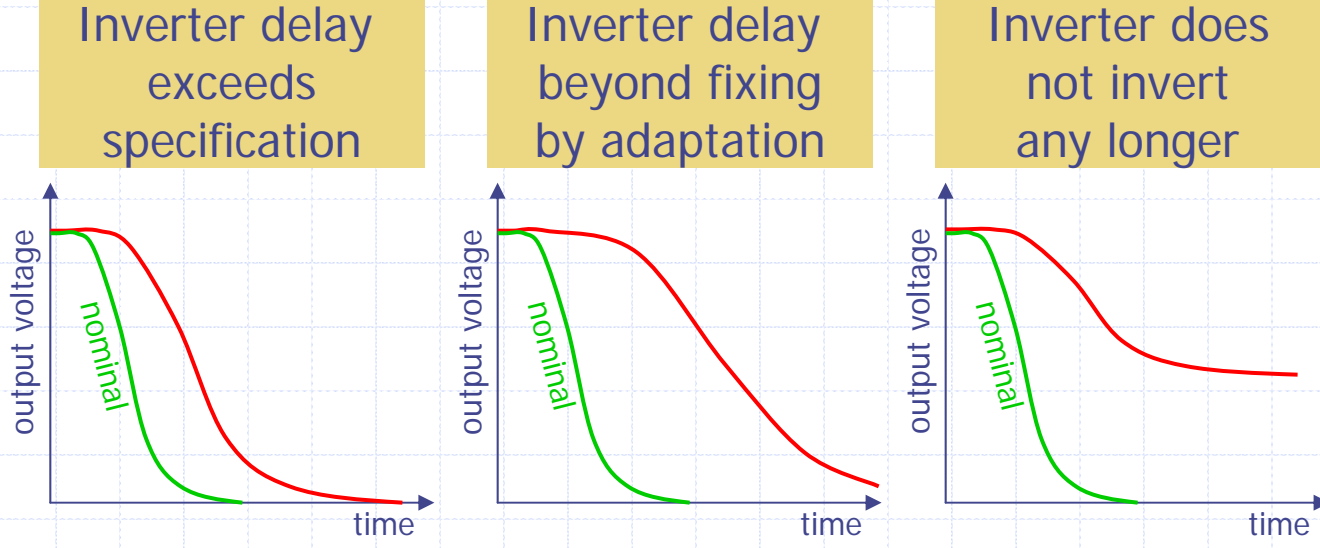
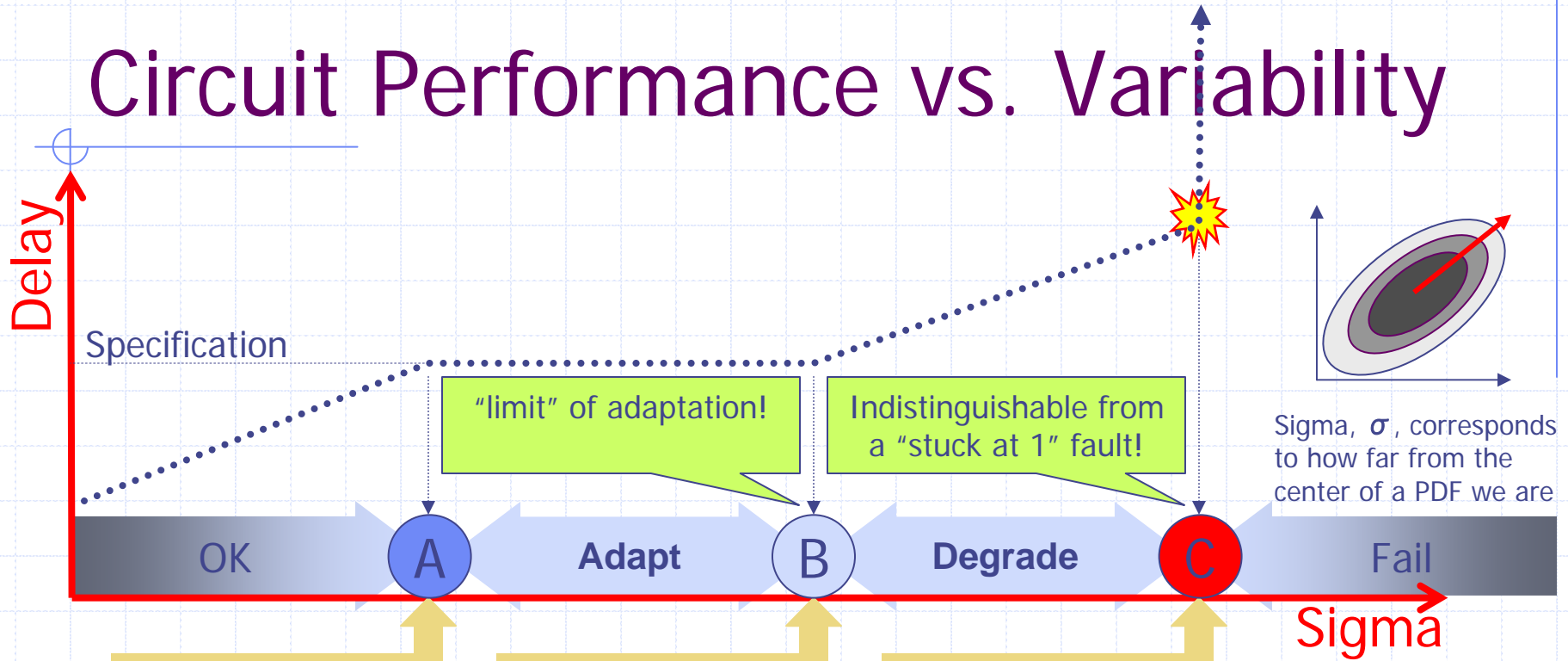
# One Possible Starting Point

- ◆ Variability increases as we shrink devices.
- ◆ Noise increases (as a %) as we shrink circuits.
  - Intrinsic, e.g. shot, thermal, coupling, etc...
  - Extrinsic, e.g. energetic particles.
  
- ◆ To combat errors we can:
  - Innovate in the circuit domain.
  - Innovate in the materials domain.
  - Spend more power and/or Si area.
  - Innovate in the micro-architecture domain.
  - Innovate in the application/software domain.

# A Study I Would Like to Extend

- ◆ The following study was done at IBM a while back on canonical components of a chip.
  - Buffer, Latch and SRAM cell.
- ◆ It is based on IBM models and circuits.
  - Difficult to share.
- ◆ Will create an open source (PTM based?) implementation that would allow broader application.
- ◆ Will extend to include additional sources of noise.

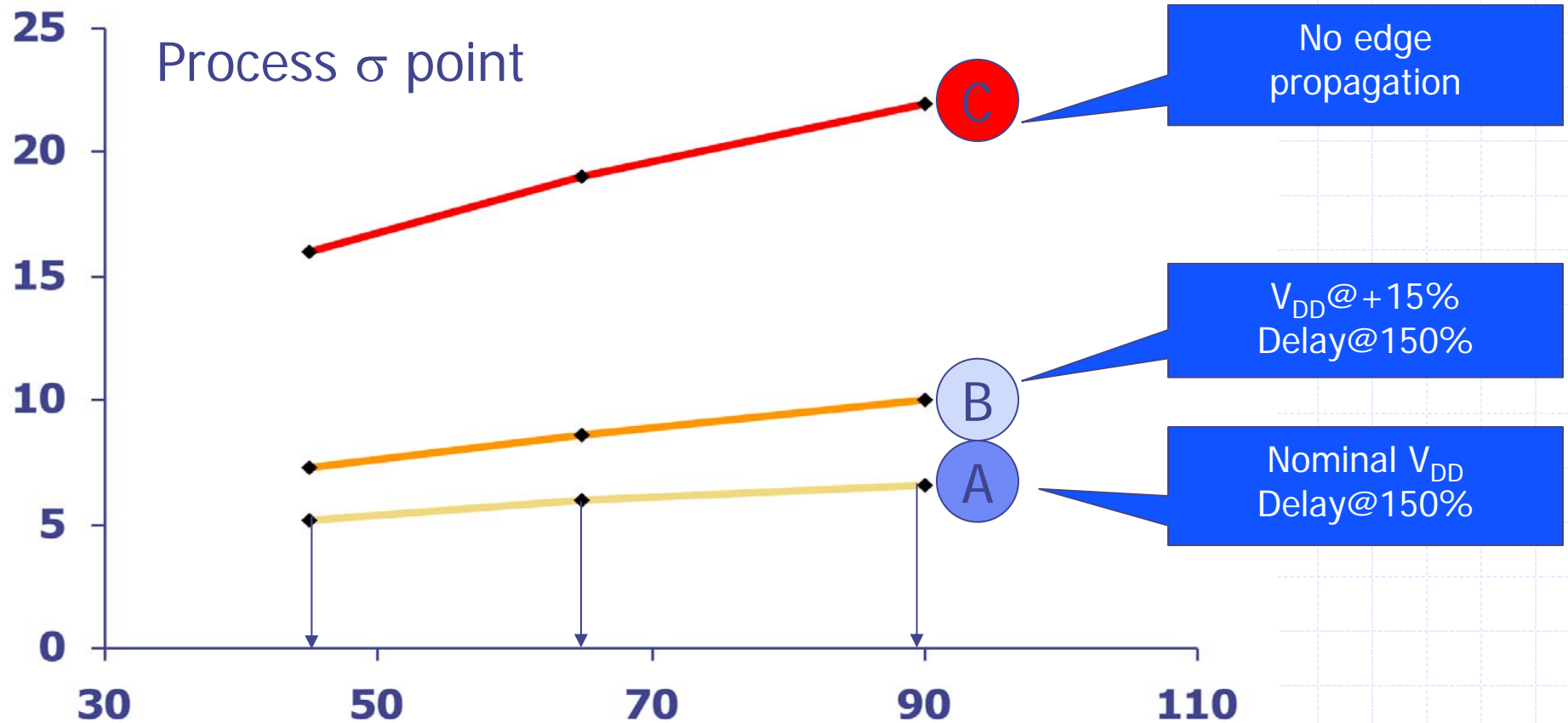
# Circuit Performance vs. Variability





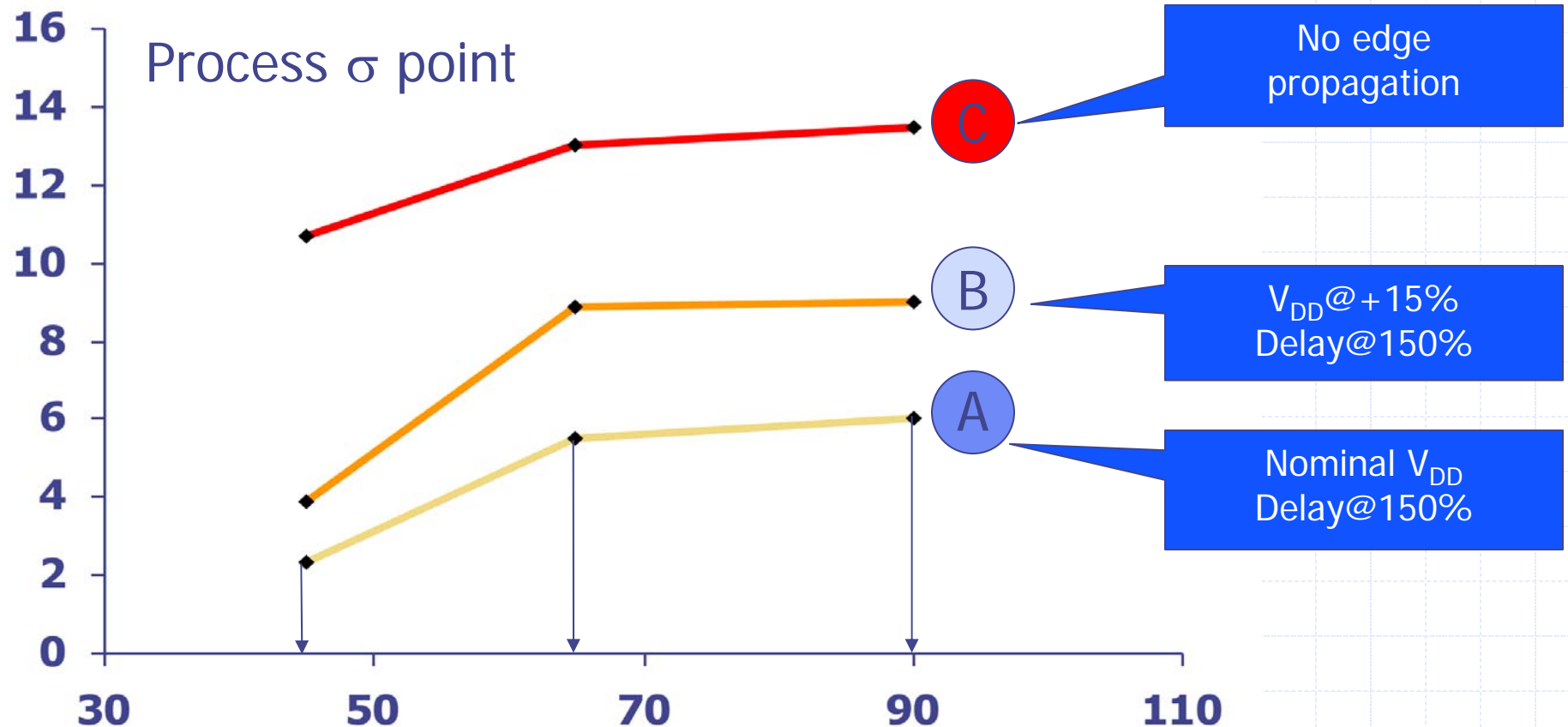
# Trend For a Simple Buffer

- ◆ Simplest possible circuit (if this fails, everything else will).
- ◆ Performed analysis for 90nm, 65nm and 45nm.
- ◆ Clear trend in sigma!



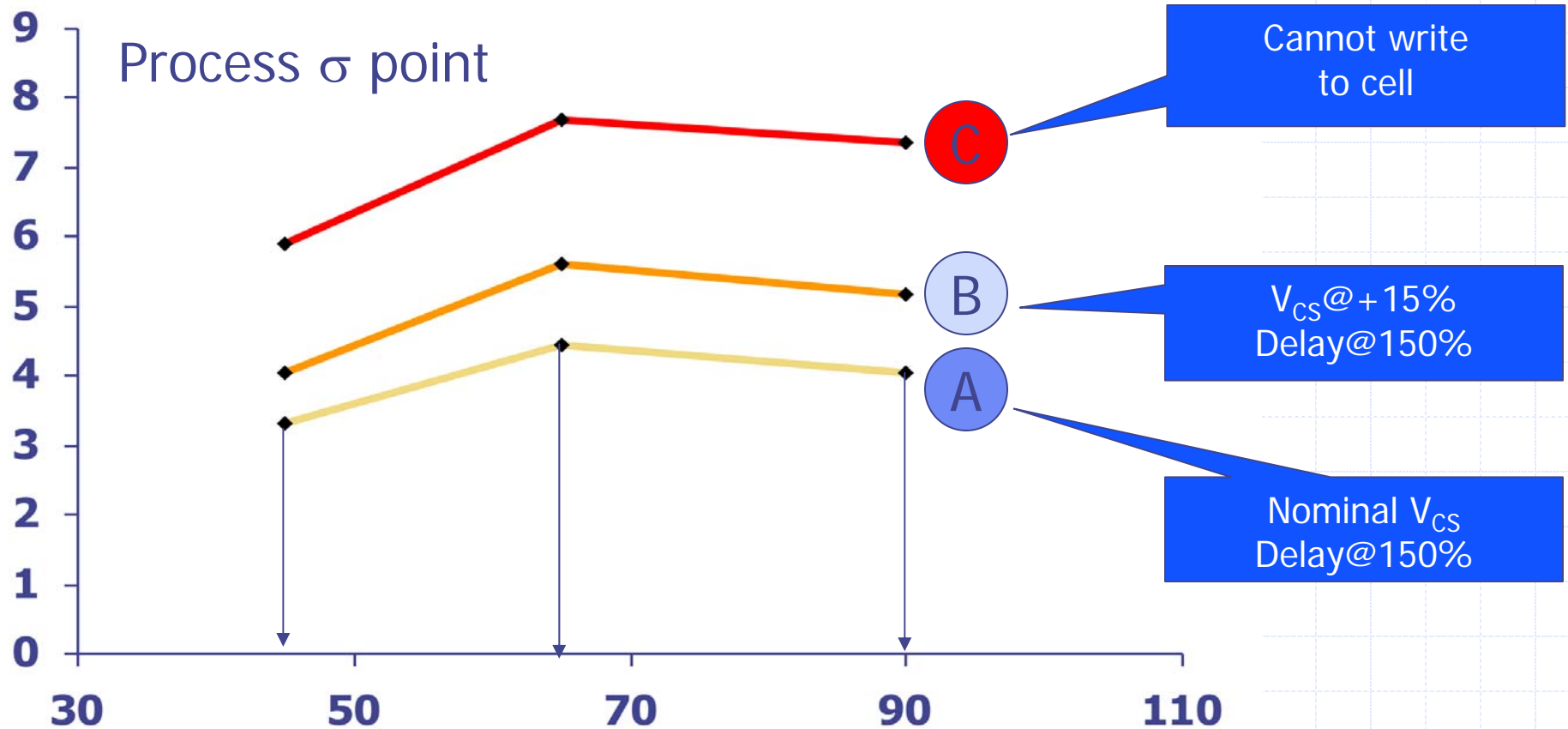
# Technology Trend For a Simple Latch

- ◆ Pervasive circuit crucial for correct logic operation.
- ◆ Performed analysis for 90nm, 65nm and 45nm.
- ◆ Clear trend in sigma!



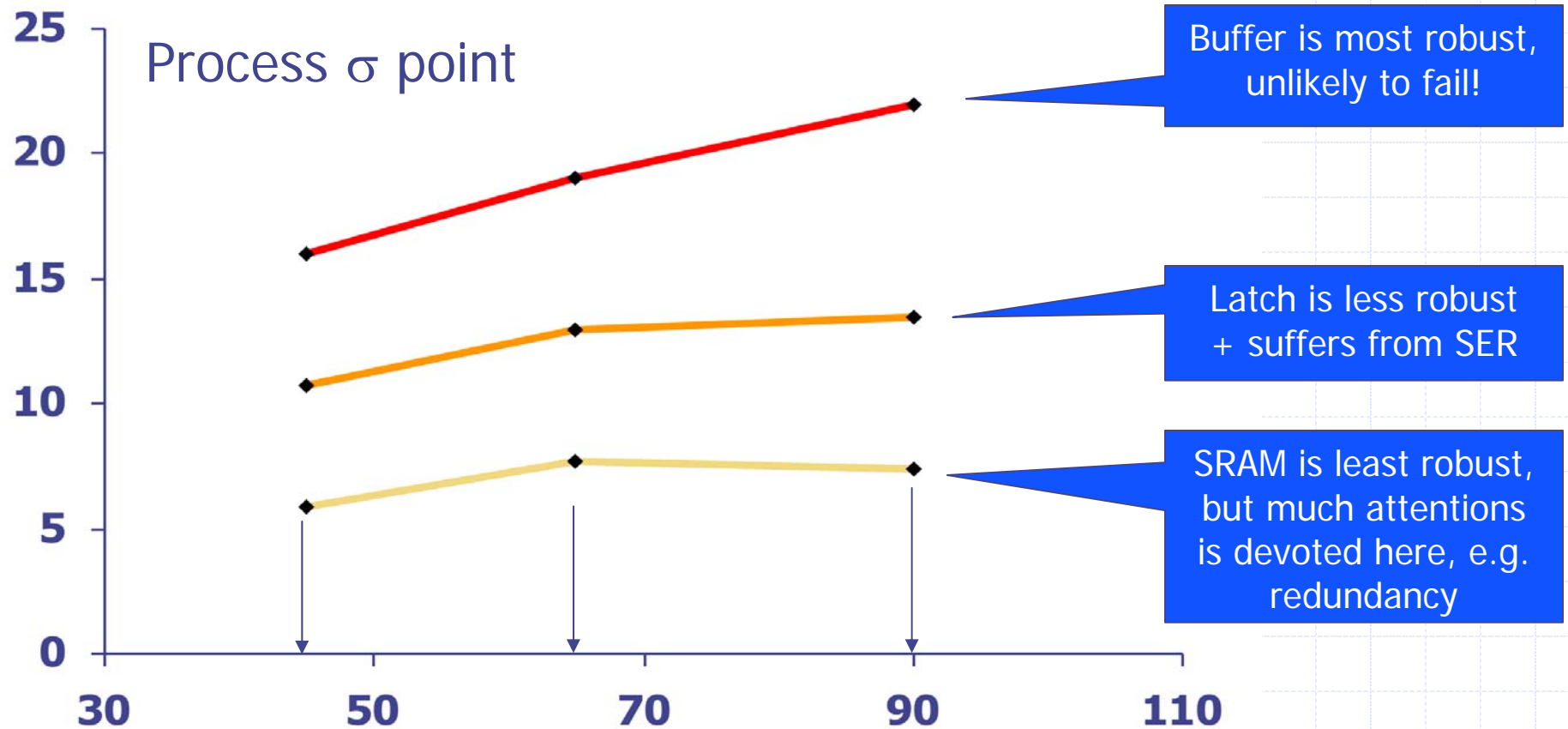
# Technology Trend for an SRAM

- ◆ SRAM is known to be a more sensitive circuit... (lower  $\sigma$ ).
- ◆ But, circuit heavily optimized for each technology.
- ◆ Much lower  $\sigma$  values + similar trend in sigma!



# Comparison of Circuits (@Point C)

- ◆ Global trend remains clear, few generations left?
- ◆ Technology trend is modulated by circuit innovation and investment in analysis and optimization tools.



# Final Thoughts

- ◆ Feedback on plan is greatly appreciated.
- ◆ Suggestions for people to include in the team (including students) welcome.
- ◆ Suggestions for future broadening of the plan to include other areas also welcome.
- ◆ Any time during this meeting, or via email.