Reliable Aerospace Computing

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Slide 1

Aerospace Computing

Covers a wide range of missions

- Computer-assisted avionics
- Deployed data processing systems
- Increasing need for autonomous computing, especially in the national security sector
 - Battery-powered
 - Harsh environments: radiation, temperature, weather
 - Little to no operator interaction



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Satellite Deployed Data Processing

- In recent years, the US's national security mission has focused on ubiquitous surveillance of targets and interests to provide an overall reduction of global threats
 - This data plays an important role in national security and policy decisions
- Many sensors, many platforms, a lot of data
 - Automating data processing important
- Satellite mission requirements can vary:
 - Experiments with flexible availability
 - Operational systems with five minutes of downtime and two ground interventions per year
 - Operational systems that are expected to survive nuclear events for measurement and detection purposes



http://mars.jpl.nasa.gov/mgs/gallery/images/mgs-mons.jpg



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Designing Satellite Systems

- Very harsh, dynamic radiation environment of heavy ions and protons based on orbit and solar cycle
 - More radiation that terrestrial environment
 - Electronics affected by both the accumulation of dose (total dose) and individual ions (single event effects)
 - Heavy ion susceptibilities are 5-7 orders of magnitude worse than proton/neutron sensitivities
- Temperature variations can be difficult
 - Rapid temperature swings multiple times a day enhance aging effects
 - Radiation effects can be enhanced as temperature increases



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Slide 4

The State of Space Electronics

- Rad-hard technology tends to be older, slower, larger, more expensive
- "Rad-Hard" is not what it used to be:
 - Onset thresholds for single-event upsets and single-event latchup lowering
 - Devices are increasing in size causing an increase in per-device cross-section
 - Single-event transients problems are increasing with feature shrink

Waiting for a better memory solution:

- RHBP memories: old, slow, small, not completely SEU-immune
- Flash memories: very low total dose
- Commercial memories: single-event latchup, B10 contamination, very high MBU rate, high current contention issues in "unscrubbable" areas of the device





Dodd, et. Al., "Impact of Heavy Ion Energy and Nuclear Interactions on Single-Event Upset and Latchup in Integrated Circuits." IEEE Transactions on Nuclear Science (Dec. 2007) vol.54, no.6, p. 2303-11

Slide 5





A Partial Space Solution...Fly Commercial

- SRAM FPGAs from Xilinx are making inroads
- A number of mitigation methods were explored
 - Spatially redundant modules: TMR, partial TMR, DWC, partial DWC
 - Quadded logic
 - State machine encoding
 - Temporal TMR
 - Everything but spatially redundant modules decreased the reliability of the circuit
- POL, ADC, and memory devices becoming challenging
- Industry partnership necessary



Cibola Flight Experiment



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Airplane Systems

- Airplane-based computational systems are increasingly important – not just for avionics but for deployed data processing also
 - Larger cargo planes can house a small supercomputer with several sensors
 - Mission requirements not well quantified yet
- Radiation environment is less harsh than space environment, but much harsher than sea level radiation rates
 - Constant flux of protons and neutrons
 dependent on location and solar cycle
 - High altitudes and near poles can see 100-1000 times more radiation per hour than at sea level
- Temperature variations still difficult







The State of Airplane-based Systems

Problem is not solved:

- Limited test data on neutron sensitivities
- Limited knowledge of the radiation environment both external and internal to the airplane
- The larger system size could drive a need to mitigate radiation-induced issues
 - Do we need to do space-level mitigation or can we scale back mitigation?
 - Current clamping for single-event latchup: no idea how quickly the system needs to be clamped, no idea on the amount of latent damage that occurs before it is clamped, no idea how that affects the mission
 - Hamming codes with data striping across memories so that entire memories can
 go down and be restored
 - Mitigating both FPGA circuits and software to single-event transients and singleevent upsets, and deliberately sparing cores for redundancy



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Things to Keep in Mind

Are existing problems "solved"

- The theory for memory correction is old, but in practice very hard to implement with current devices
- The theory for correcting data communication errors is old, but in practice making very high speed communication reliable in a very high fault rate environments not well studied

Can we build systems that can seamlessly adapt to different types of environments?

- With different error rates?
- With different mission requirements?
- Without a not complete understanding of the defect/failure models?
- Without completely redesigning the entire system?
- What is the granularity to solve reliability problems?
 - Can we avoid solving the component problem by addressing a system solution?
 - How do we best handle error filtering?



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